What is claimed is:

1. A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal and a drain terminal configured to output a signal corresponding to said controlled signal; and

an inductor element provided between a source terminal and a ground terminal of said FET,

wherein an inductance value of said inductor element is set so that said inductor element resonates in series for a reactance component of a gate-to-source impedance by said controlled signal when a drain voltage of said FET is lower than a source voltage thereof.

2. A semiconductor integrated circuit as set forth in claim 1, which further comprises a second capacitor element provided between the gate terminal and the source terminal of said FET,

wherein a capacitance value of said second capacitor element is set so that a parasitic resistance component of said FET apparently decreases when the drain voltage of said FET is lower than the source voltage thereof.

3. A semiconductor integrated circuit as set forth in claim 1, which further comprises a third capacitor element provided between the drain terminal and the source terminal of said FET,

wherein a capacitance value of said third capacitor element is set so that a parasitic resistance component of said FET apparently decreases when the drain voltage of said FET is lower than the source voltage thereof.

4. A semiconductor integrated circuit as set forth in claim 1, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to switch and controlling the magnitude relationship between the drain voltage and the source voltage of said FET.

5. A semiconductor integrated circuit as set forth in claim 2, which further comprises a control signal input circuit,

connected to the drain terminal of said FET, configured to switch and controlling the magnitude relationship between the drain voltage and the source voltage of said FET.

6. A semiconductor integrated circuit as set forth in claim 3, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to switch and controlling the magnitude relationship between the drain voltage and the source voltage of said FET.

7. A semiconductor integrated circuit as set forth in claim 4, wherein said control signal input circuit sets a drain-to-source voltage so that Cgd / (Cgd + Cgs) · Rds / (Rds + RL), which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

8. A semiconductor integrated circuit as set forth in claim 5, wherein said control signal input circuit sets a drain-to-source voltage so that Cgd / (Cgd + Cgs) · Rds / (Rds + RL), which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

9. A semiconductor integrated circuit as set forth in claim 6, wherein said control signal input circuit sets a drain-to-source voltage so that Cgd / (Cgd + Cgs) · Rds / (Rds + RL), which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

10. A semiconductor integrated circuit as set forth in claim 1, which further comprises a bias supply circuit configured to supply a dc bias voltage to at least one of the gate terminal,

drain terminal and source terminal of said FET.

11. A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal and a drain terminal configured to output a signal corresponding to said controlled signal; and

an inductor element and a first capacitor element which are connected to each other in series between a source terminal and a ground terminal of said FET,

wherein an inductance value of said inductor element is set so that said inductor element resonates in series for a reactance component of a gate-to-source impedance by said controlled signal when a drain voltage of said FET is lower than a source voltage thereof.

12. A semiconductor integrated circuit as set forth in claim 11, which further comprises a second capacitor element provided between the gate terminal and the source terminal of said FET,

wherein a capacitance value of said second capacitor element is set so that a parasitic resistance component of said FET apparently decreases when the drain voltage of said FET is lower than the source voltage thereof.

13. A semiconductor integrated circuit as set forth in claim 11, which further comprises a third capacitor element provided between the drain terminal and the source terminal of said FET,

wherein a capacitance value of said third capacitor element is set so that a parasitic resistance component of said FET apparently decreases when the drain voltage of said FET is lower than the source voltage thereof.

14. A semiconductor integrated circuit as set forth in claim 11, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to switch and controlling the magnitude relationship between the drain voltage and the source voltage of said FET.

15. A semiconductor integrated circuit as set forth in claim 12, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to switch and controlling the magnitude relationship between the drain voltage and the source voltage of said FET.

16. A semiconductor integrated circuit as set forth in claim 13, which further comprises a control signal input circuit, connected to the drain terminal of said FET, configured to switch and controlling the magnitude relationship between the drain voltage and the source voltage of said FET.

17. A semiconductor integrated circuit as set forth in claim 14, wherein said control signal input circuit sets a drain-to-source voltage so that Cgd / (Cgd + Cgs) · Rds / (Rds + RL), which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

18. A semiconductor integrated circuit as set forth in claim 15, wherein said control signal input circuit sets a drain-to-source voltage so that Cgd / (Cgd + Cgs) · Rds / (Rds + RL), which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

19. A semiconductor integrated circuit as set forth in claim 16, wherein said control signal input circuit sets a drain-to-source voltage so that Cgd / (Cgd + Cgs) · Rds / (Rds + RL), which is a function of the gate-to-drain capacity Cgd, gate-to-source capacity Cgs, drain-to-source resistance Rds and load resistance RL of said FET, is minimum when the drain voltage of said FET is lower than the source voltage thereof.

20. A semiconductor integrated circuit as set forth in claim

11, which further comprises a bias supply circuit configured to supply a dc bias voltage to at least one of the gate terminal, drain terminal and source terminal of said FET.